FORM PTO-1449 INFORMATION DISCLOSURE STATEMENT	ATTY. DOCKET NO. 1875.2830002/RES/GSB	APPLICATION NO. *To Be Assigned* 10684444
	APPLICANTS Mulder *et al.*	
	FILING DATE *Herewith*	GROUP *To Be Assigned*

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA1	3,846,712	11/1974	Kiko	330	30	
	AB1	4,959,563	09/1990	Schenck	326	32	
	AC1	5,006,727	04/1991	Ragosch *et al.*	327	65	
	AD1	5,118,971	06/1992	Schenck	326	32	
	AE1	5,157,397	10/1992	Vernon	341	157	
	AF1	5,191,336	03/1993	Stephenson	341	111	
	AG1	5,302,869	04/1994	Hosotani *et al.*	307	518	
	AH1	5,471,210	11/1995	Wingender *et al.*	341	156	
	AI1	5,554,943	09/1996	Moreland	327	65	
	AJ1	5,867,116	02/1999	Nakamura *et al.*	341	159	
	AK1	5,973,632	10/1999	Tai	341	156	

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL1						Yes No
	AM1						Yes No
	AN1						Yes No
	AO1						Yes No
	AP1						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

AR	1	Abo, A.M. and Gray, P.R., "A 1.5-V, 10-bit, 14.3-MS/s CMOS Pipeline Analog-to-Digital Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 5, May 1999, pp. 599-606.
AS	1	Brandt, B.P. and Lutsky, J., "A 75-mW, 10-b, 20-MSPS CMOS Subranging ADC with 9.5 Effective Bits at Nyquist," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 12, December 1999, pp. 1788-1795.
AT	1	Bult, Klaas and Buchwald, Aaron, "An Embedded 240-mW 10-b 50-MS/s CMOS ADC in 1-mm²," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 32, No. 12, December 1997, pp. 1887-1895.

EXAMINER	DATE CONSIDERED 4/12/04

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA2	6,259,745	07/2001	Chan	375	285	
	AB2	6,489,913	12/2002	Hansen *et al.*	341	156	
	AC2						
	AD2						
	AE2						
	AF2						
	AG2						
	AH2						
	AI2						
	AJ2						
	AK2						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL2						Yes No
	AM2						Yes No
	AN2						Yes No
	AO2						Yes No
	AP2						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	2	Cho, T.B. and Gray, P.R., "A 10 b, 20 Msample/s, 35 mW Pipeline A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 3, March 1995, pp. 166-172.
	AS	2	Choe, M-J. et al., "A 13-b 40-Msamples/s CMOS Pipelined Folding ADC with Background Offset Trimming," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 12, December 2000, pp. 1781-1790.
	AT	2	Choi, M. and Abidi, A., "A 6-b 1.3-Gsample/s A/D Converter in 0.35-μm CMOS," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 36, No. 12, December 2001, pp. 1847-1858.

EXAMINER	DATE CONSIDERED 8/12/04

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA3						
	AB3						
	AC3						
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	AE3						
	AF3						
	AG3						
	AH3						
	AI3						
	AJ3						
	AK3						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL3						Yes No
	AM3						Yes No
	AN3						Yes No
	AO3						Yes No
	AP3						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	3	Dingwall *et al.*, IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 6, "An 8-MHz CMOS Subranging 8-Bit A/D Converter", December 1985, pgs. 1138-1143
	AS	3	Flynn, M. and Sheahan, B., "A 400-Msample/s, 6-b CMOS Folding and Interpolating ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 33, No. 12, December 1998, pp. 1932-1938.
	AT	3	Geelen, G., "A 6b 1.1GSample/s CMOS A/D Converter," IEEE International Solid-State Circuits Conference, IEEE, 2001, pp. 128-129 and 438.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA4						
	AB4						
	AC4						
	AD4						
	AE4						
	AF4						
	AG4						
	AH4						
	AI4						
	AJ4						
	AK4						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL4						Yes No
	AM4						Yes No
	AN4						Yes No
	AO4						Yes No
	AP4						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	4	Hoogzaad, G. and Roovers, R., "A 65-mW, 10-bit, 40-Msample/s BiCMOS Nyquist ADC in 0.8 mm²," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 12, December 1999, pp. 1796-1802.
	AS	4	Hosotani, S. et al., "An 8-bit 20-MS/s CMOS A/D Converter with 50-mW Power Consumption," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 25, No. 1, February 1990, pp. 167-172.
	AT	4	Ingino, J.M. and Wooley, B.A., "A Continuously Calibrated 12-b, 10-MS/s, 3.3-V A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 33, No. 12, December 1998, pp. 1920-1931.

EXAMINER	DATE CONSIDERED 8/12/04

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA5						
	AB5						
	AC5						
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	AI5						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL5						Yes No
	AM5						Yes No
	AN5						Yes No
	AO5						Yes No
	AP5						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	5	Ito, M. et al., "A 10 bit 20 MS/s 3 V Supply CMOS A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 29, No. 12, December 1994, pp. 1531-1536.
	AS	5	Kattman, K. and Barrow, J., "A Technique for Reducing Differential Non-Linearity Errors in Flash A/D Converters," *IEEE International Solid-State Conference*, IEEE, 1991, pp. 170-171.
	AT	5	Kusumoto, K. et al., "A 10-b 20-MHz 30-mW Pipelined Interpolating CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 28, No. 12, December 1993, pp. 1200-1206.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA6						
	AB6						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL6						Yes No
	AM6						Yes No
	AN6						Yes No
	AO6						Yes No
	AP6						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	6	Lewis, S. et al., "A 10-b 20-Msample/s Analog-to-Digital Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 27, No. 3, March 1992, pp. 351-358.
	AS	6	Mehr, I. and Singer, L., "A 55-mW, 10-bit, 40-Msample/s Nyquist-Rate CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 3, March 2000, pp. 318-325.
	AT	6	Miyazaki *et al.*, ISSCC 2002/Session 10/High-Speed ADCs/10.5, "A 16mW 30MSample/s 10b Pipelined A/D Converter using a Pseudo-Differential Architecture", February 5, 2002, 3 pgs.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA7						
	AB7						
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	AI7						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL7						Yes No
	AM7						Yes No
	AN7						Yes No
	AO7						Yes No
	AP7						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	7	Nagaraj, K. et al., "Efficient 6-Bit A/D Converter Using a 1-Bit Folding Front End," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 8, August 1999, pp. 1056-1062.
	AS	7	Nagaraj, K. et al., "A Dual-Mode 700-Msamples/s 6-bit 200-Msamples/s 7-bit A/D Converter in a 0.25-μm Digital CMOS," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 12, December 2000, pp. 1760-1768.
	AT	7	Nauta, B. and Venes, A., "A 70-MS/s 110-mW 8-b CMOS Folding and Interpolating A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 12, December 1995, pp. 1302-1308.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA8						
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FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL8						Yes No
	AM8						Yes No
	AN8						Yes No
	AO8						Yes No
	AP8						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	8	Pan, H. et al., "A 3.3-V 12-b 50-MS/s A/D Converter in 0.6-μm CMOS with over 80-dB SFDR," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 12, December 2000, pp. 1769-1780.
	AS	8	Song, W-C. et al., "A 10-b 20-Msample/s Low-Power CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 5, May 1995, pp. 514-521.
	AT	8	Sumanen, L. et al., "A 10-bit 200-MS/s CMOS Parallel Pipeline A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 36, No. 7, July 2001, pp. 1048-1055.

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U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA9						
	AB9						
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	AD9						
	AE9						
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	AG9						
	AH9						
	AI9						
	AJ9						
	AK9						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL9						Yes No
	AM9						Yes No
	AN9						Yes No
	AO9						Yes No
	AP9						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	9	Sushihara *et al.*, ISSCC 2002/Session 10/High-Speed ADCs/10.3, "A 7b 450MSample/s 50mW CMOS ADC in 0.3 mm², February 5, 2002, 3 pgs.
	AS	9	Taft, R.C. and Tursi, M.R., "A 100-MS/s 8-b CMOS Subranging ADC with Sustained Parametric Performance from 3.8 V Down to 2.2 V," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 36, No. 3, March 2001, pp. 331-338.
	AT	9	van der Ploeg, H. and Remmers, R., "A 3.3-V, 10-b 25-Msample/s Two-Step ADC in 0.35-μm CMOS," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 34, No. 12, December 1999, pp. 1803-1811.

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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA10						
	AB10						
	AC10						
	AD10						
	AE10						
	AF10						
	AG10						
	AH10						
	AI10						
	AJ10						
	AK10						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL10						Yes No
	AM10						Yes No
	AN10						Yes No
	AO10						Yes No
	AP10						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	10	van der Ploeg, H. et al., "A 2.5-V 12-b 54-Msample/s 0.25-μm CMOS ADC in 1-mm^2 With Mixed-Signal Chopping and Calibration," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 36, No. 12, December 2001, pp. 1859-1867.
	AS	10	Vorenkamp, P. and Roovers, R., "A 12-b, 60-Msample/s Cascaded Folding and Interpolating ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 32, No. 12, December 1997, pp. 1876-1886.
	AT	10	Wang, Y-T. and Razavi, B., "An 8-bit 150-MHz CMOS A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 35, No. 3, March 2000, pp. 308-317.

EXAMINER	DATE CONSIDERED
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EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB-CLASS	FILING DATE
	AA11						
	AB11						
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	AG11						
	AH11						
	AI11						
	AJ11						
	AK11						

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION
	AL11						Yes No
	AM11						Yes No
	AN11						Yes No
	AO11						Yes No
	AP11						Yes No

OTHER (Including Author, Title, Date, Pertinent Pages, etc.)

	AR	11	Yotsuyanagi, M. et al., "A 2 V, 10 b, 20 Msample/s, Mixed-Mode Subranging CMOS A/D Converter," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 30, No. 12, December 1995, pp. 1533-1537.
	AS	11	Yu, P.C. and Lee, H-S., "A 2.5-V, 12-b, 5-Msample/s Pipelined CMOS ADC," *IEEE Journal of Solid-State Circuits*, IEEE, Vol. 31, No. 12, December 1996, pp. 1854-1861.
	AT	11	

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